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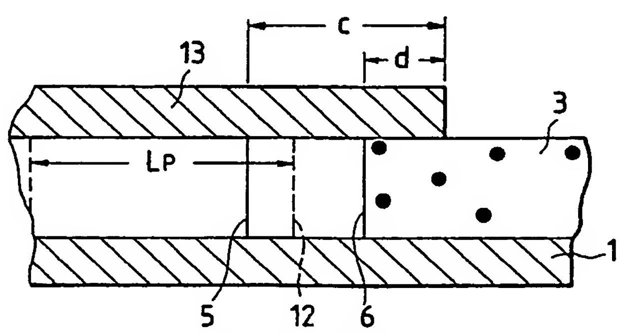
## (54) Semiconductor commutator.

(57) A semiconductor commutator (Fig.4) which is constructed by providing a semiconductor region of a first conductivity type (3) and a semiconductor region of a second conductivity type, wherein there is provided a grain boundary (5) which is located near a junction surface (6) of the semiconductor region of the first conductivity type (3) and the semiconductor region of the second conductivity type so as not to cross said junction surface (6). The commutator may be manufactured by using a technique of selective nucleation and growth.

FIG. 4




EP 0 367 446 A1

# Semiconductor Commutator

## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates to a semiconductor commutator and. more particularly, to a semiconductor commutator which is constructed by joining a semiconductor region of the first conductivity type and a semiconductor region of the second conductivity type.

### Related Background Art

In a PN junction diode, improvement in switching speed is strongly demanded. However, in a PN junction diode using a monocrystal, since a carrier life time in bulk is long, when switching from the ON state to the OFF state, excessive minority carriers remain, so that the delay time for switching becomes long and there is a limitation in improvement of the switching speed.

Hitherto, in order to improve the switching speed, heavy metal, for instance, gold is used as a recombination center for a PN diode or a PN junction diode is formed on a polycrystalline semiconductor layer and a grain boundary defect is used as a recombination center, thereby reducing the life time of the minority carriers and decreasing the delay time.

However, in the above conventional example, in the case of using gold as a recombination center, there is a problem such that field concentration occurs in gold atoms. On the other hand, in the case of using a grain boundary defect as a recombination center, there is a problem such that since impurities are segregated in the grain boundary near a high concentration layer, field concentration occurs in the grain boundary which crosses the junction surface.

Thus, electric field breakdown occurs and a dark current component increases from a grain boundary within a depletion layer as a generation center. That is, since a particle size of polycrystalline silicon is very small, there is no limitation in a position of the particles. Therefore, when the boundary defect is used as the recombination center, the position of the grain boundary is optional one within whole element.

Many boundaries are within and in the vicinity of the high concentration layer. As a result, at the grain boundary, impurities are segragated, which adversely effects the element property. Such phenomena will now be practically described.

Fig. 1 shows the current to voltage characteristics of a PN junction diode. In the diagram, a solid curve indicates the ideal preferable characteristics. However, actually, since a dark current component is caused due to the electric field breadkown, the characteristics become as shown by a broken line.

## SUMMARY OF THE INVENTION

An object of the present invention is to provide a semiconductor commutator capable of high speed operation and an excellent current-voltage property.

Another object of the present invention is to provide a semiconductor commutator which is constructed by joining a semiconductor region of the first conductivity type and a semiconductor region of the second conductivity type, wherein a grain boundary is provided near the junction surface of the semiconductor region of the first conductivity type and the semiconductor region of the second conductivity type so as not to cross the junction surface.

A semiconductor commutator of the invention exhibits the good current to voltage characteristics in which the commutator can operate at a high speed and the life time of minority carriers is reduced by effectively using a grain boundary defect, as a recombination center, in which a grain boundary is arranged between a junction surface and an electrode so as not to cross the junction surface.

Still another object of the present invention is to provide a commutator wherein a crystal forming process is executed to a substrate having a non-nucleus forming surface whose nucleus forming density is small and a free surface which has an enough small area so that only a single nucleus to be grown into single crystal is formed and on which a plurality of nucleus forming surfaces each having a nucleus forming density larger than the nucleus forming density of said non-nucleus forming surface are adjacently arranged at a predetermined distance away from one another, a monocrystal is grown from the single nucleus of each of said plurality of nucleus forming surfaces which are arranged at the predetermined distance away from one another, and the grain boundary is formed at the position where said monocrystals are joined.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a graph showing the current to voltage characteristics of a PN junction diode:

Fig. 2 is a schematic partial cross sectional view for explaining a construction of a semiconductor commutator of an embodiment 1 of the invention:

Fig. 3 is a schematic partial plan view of the semiconductor commutator:

Fig. 4 is a schematic partial cross sectional view for explaining an arrangement of a grain boundary of the semiconductor commutator;

Figs. 5A to 5E are respectively schematic vertical sectional views showing manufacturing steps to form a crystal substrate which is used in the semiconductor commutator of the embodiment of the invention;

Fig. 6 is a schematic perspective view showing an $Si_3N_4$ film formed on an $SiO_2$ film;

Fig. 7 is a schematic partial plan view showing a construction of a semiconductor commutator of an embodiment 2 of the invention;

Fig. 8 is a schematic partial plan view showing a wiring state of the semiconductor commutator of the embodiment 2 of the invention; and

Fig. 9 is a circuit diagram showing a circuit which is used to measure a recovery time in the reverse direction of the semiconductor commutator of the embodiment of the invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the invention will be described in detail hereinbelow with reference to the drawings.

First, manufacturing steps to form a crystal substrate having a grain boundary which is used in a semiconductor commutator of the embodiment of the invention will be described.

For instance, a crystal growing method disclosed in E.P. Application Publication No. 0,244,081 can be used.

Figs. 5A to 5E are vertical sectional views showing an example of the manufacturing steps to form a crystal substrate which is used in the semiconductor commutator in the embodiment of the invention.

Fig. 6 is a perspective view showing an $Si_3N_4$ film formed on an $SiO_2$ film and corresponds to the manufacturing step shown in Fig. 5A.

First, as shown in Figs. 5A and 6, $SiO_2$ film 1 having a thickness of 2000 Å serving as a non-nucleus forming surface is formed on a silicon wafer of (100) by using a thermal oxidation process. An $Si_3N_4$ film of 300 Å is deposited onto the $SiO_2$ film 1. Further, the $Si_3N_4$ film is patterned by using a well-known fine processing technique in a manner such that nuclei each having a size of 2 µm□ are arranged at an interval b (in this case, b = 100 µm). A resultant $Si_3N_4$ film 8 serving as a nucleus forming surface which was formed is hereinafter called a site.

Next, as shown in Fig. 5B, by executing a vapor phase growing process of the $SiH_2Cl_2$ $H_2$ $PH_3$ system, a crystal nucleus of Si can be formed only in the site 8 since the nucleus forming concentration of $Si_3N_4$ is larger than that of $SiO_2$. If the size of the site 8 is set to be sufficiently small, only one crystalline nucleus 9 of Si to be grown into single crystalline silicon can be formed in the single site 8.

Next, as shown in Fig. 5C, when crystal is subsequently grown, only one crystalline nucleus 9 on each site 8 continuously grows, an Si monocrystalline grain 10 is formed, and the Si monocrystalline grain 10 can be further grown.

Next, as shown in Fig. 5D, the Si monocrystalline grains 10 which grew from both of the adjacent sites 8 are joined at the center between the sites 8, thereby forming a grain boundary 11. As shown in the diagram, the grain boundary 11 is formed in the direction perpendicular to the substrate.

Then, as shown in Fig. 5E, the substrate on which the grain boundary 11 was formed by joining the Si monocrystalline grains 10 is ground until a thickness of crystalline layer becomes 2 µm, thereby forming a monocrystalline layer 2. Thus, an n type silicon crystalline substrate in which the position of the grain boundary was controlled like a lattice of an interval of 100 µm and a phosphorus (P) concentration is set to $1 \times 10^{16}$ atom/cm$^3$ was obtained.

In the invention, the crystalline substrate in which the position of the grain boundary was controlled is a significant component member and, preferably, it can be formed by using the crystal growing method disclosed in the E.P. Application Publication No. 0,244,081 mentioned above. However, the invention is not limited to such a method but any other preferable methods can be also used, if a grain boundary position can be controlled by the methods.

The semiconductor commutator of the invention can be manufactured as follows by using the n type silicon crystalline substrate formed by th manufacturing steps described above.

(Embodiment 1)

Fig. 2 is a partial cross sectional view for explaining a construction of a semiconductor commutator of the embodiment 1 of the invention.

Fig. 3 is a partial plan view of the semiconductor commutator.

Fig. 4 is a partial cross sectional view for

explaining an arrangement of a grain boundary of the semiconductor commutator.

First, on the n type silicon crystalline substrate, $SiO_2$ film with a thickness of 5000 Å is formed. Next, in order to form high impurity concentration region within only a desired single crystal grain in the single crystal layer 2, a portion of the $SiO_2$ film corresponding to the single crystalline grain is removed. In the present embodiment, the portion of $SiO_2$ 93 µm square was removed. Next, using $SiO_2$ film as a mask, BN diffusion is conducted at a temperature 100°C for 2 hours, thereby an impurity diffusion layer is extend to under layer (silicon wafer in the present embodiment). A high impurity p type semiconductor region 3 as shown in Fig. 2 is formed. The state of this is described with reference to Fig. 4 as follows.

In Fig. 4, reference numeral 13 denotes a BN diffused oxide film for masking. c indicates a distance from a grain boundary 5 to the edge portion of the $SiO_2$ film (in this case, about 3.5 µm) and d represents a distance of the diffusion in the lateral direction by the BN diffusion (in this case, about 1.4 µm and corresponds to about 70 % of the depth). The main surface on which the p type semiconductor region 3 and an n type semiconductor region 2a were ground and the grain boundary 5 are perpendicularly formed almost in parallel with a junction surface 6.

In order to form an $n^+$ type semiconductor region 4 to come into contact with the n type monocrystalline grain (n type semiconductor region 2a) adjacent to the monocrystalline grain in which the $p^+$ type semiconductor region 3 is formed, a thermal oxide film having a thickness of 4000 Å is formed. Thereafter, the $SiO_2$ film is selectively eliminated, a PSG film having a thickness of 4000 Å is deposited by an A-CVD process, a heat treatment is executed at 900°C for 30 minutes, and impurities (P) are diffused. As shown in Fig. 3, contact holes are formed and aluminum (Aℓ) is evaporation deposited and they are used as electrodes. An $SiO_2$ film having a thickness of 1000 Å is deposited as a protective film.

It should be noted here that, as shown in Fig. 4, the grain boundary 5 exists in a region from a depletion edge 12 to a position of a diffusion length $L_p$ ($L_p$ denotes a diffusion length of a hole). In the embodiment, the diffusion length $L_p$ is set to about up to 5 µm and the junction surface 6 exists at a position which is away from the grain boundary 5 by about 2 µm when considering also the diffusion distance d in the lateral direction due to the BN diffusion. On the other hand, since a depletion layer width is set to about 1 µm at 20 volts, as shown in Fig. 4, the grain boundary 5 is located within the diffusion length $L_p$ from the depletion edge 12.

In the embodiment, a number of excessive minority carriers exist in the region from the depletion edge 12 to the diffusion length $L_p$ and the recombination center existing in such a region most effectively functions. Therefore, even if the number of defects existing in this region is not so large, the switching operation can be executed at a high speed. That is, according to the invention, there is provided a semiconductor commutator which can operate at a high speed and has good current to voltage characteristics by effectively using a grain boundary defect, as a recombination center, in which a grain boundary is arranged between the junction surface and the electrode so as not to cross the junction surface.

It is considered that the defect level of the grain boundary defect exists at the center than 0.2 eV of gold, and the grain boundary defect functions as a more effective recombination center than gold. That is, a level which most effectively operates as the recombination center is ones at a midst of the bandgap.

A level of gold is at 0.2 eV from the midst of two bandgap, while, since the defect level of the grain boundary is at the midst, the defect energy level effectively acts as the recombination center rather than that of the gold. Since its concentration lies within a range about from $10^{12}/cm^2$ to $10^{13} cm^2$, it corresponds to $10^{17} cm^3$ or more in the case where gold is used as a recombination center. Thus, the current density in the reverse direction is set to up to $10^{-8}$ Å and this value is not so different from that of the commutator formed on the monocrystalline substrate obtained by a Cz method.

The semiconductor commutator of the embodiment exhibits the good I-V characteristics of the low dark current. An external circuit is set such that

$$\frac{I_F(V_F)}{V_R/R} \sim 100$$

by using a circuit shown in Fig. 9 and the recovery time in the reverse direction was measured. Thus, the high speed switching characteristics of up to 5 nsec were obtained.

(Embodiment 2)

The embodiment relates to the case where the semiconductor commutator in the embodiment 1 mentioned above was two-dimensionally arranged.

Fig. 7 is a partial plan view showing a construction of a semiconductor commutator in the embodiment 2 of the invention.

Fig. 8 is a partial plan view showing a wiring state of the semiconductor commutator.

As shown in Fig. 7, in the embodiment, P type semiconductor regions and N type semiconductor regions are alternately arranged like a zigzag pattern with respect to the columns and rows. Fig. 7 shows a part of the arrangement of the matrix of 10 rows x 10 columns.

The semiconductor commutator of the embodiment can be also formed by using the crystal growing method disclosed in E.P. Application Publication No. 0.244.081 in a manner similar to the embodiment 1. The $SiCl_2H_2$ $H_2$ $HCl$ system is used as a material gas system and the crystalline layer is grown until a single crystalline grain diameter becomes 50 µm. Thereafter, it is ground until a thickness of monocrystalline layer becomes 2 µm.

Then, under the conditions similar to those in the embodiment 1, after a $P^+$ layer and an $N^+$ layer were formed, contact holes and Al wirings are formed and an $SiO_2$ layer having a thickness of 10000 Å is further deposited as a protective film by a sputtering method.

In the embodiment 1, since an enough larger junction area than the area which is occupied by the device cannot be obtained, there will be a case that the embodiment 1 cannot cope with the case where a relatively large current is needed. However, in the embodiment 2, by arranging the N and P type semiconductor regions like a zigzag pattern a current value which is two or more times as large as that in the embodiment 1 can be obtained by the same area. Therefore, by using such an arrangement, a semiconductor commutator having a large junction area can be also manufactured in a small space.

The semiconductor commutator obtained in the embodiment exhibits the good I/V characteristics as shown by a solid line in Fig. 1. An external circuit is set such that the switching speed becomes.

$$\frac{I_F(V_F)}{V_R/R} \sim 100$$

by using the circuit shown in Fig. 9. The recovery time in the reverse direction was measured. Thus, the high speed switching characteristics of up to 5 nsec were obtained.

As described in detail above, according to the semiconductor commutator of the invention, it is possible to realize the semiconductor commutator in which the good I-V characteristics are obtained and the recovery time in the reverse direction has a value on the order of nsec and which can operate at a high speed.

## Claims

1. A semiconductor commutator which is constructed by providing a semiconductor region of a first conductivity type and a semiconductor region of a second conductivity type; wherein there is provided a grain boundary which is located near a junction surface of the semiconductor region of the first conductivity type and the semiconductor region of the second conductivity type so as not to cross said junction surface.

2. A commutator according to claim 1, wherein a main surface of at least one of the semiconductor region of the first conductivity type and the semiconductor region of the second conductivity type and said grain boundary are perpendicularly formed.

3. A commutator according to either claims 1 or 2, wherein said grain boundary is formed like a lattice and semiconductor regions of the first conductivity type and semiconductor regions of the second conductivity type are arranged like a zigzag pattern.

4. A commutator according to any one of the preceding claims, wherein said first conductivity type is n-type and said grain boundary is within said first conductivity type semiconductor region.

5. A commutator according to any one of the preceding claims 1 to 3, wherein said first conductivity type is n-type and said grain boundary is within said second conductivity type semiconductor region.

6. A method for producing a commutator according to any one of the preceding claims, wherein a crystal forming process is executed to a substrate having a non-nucleus forming surface whose nucleus forming density is small and a free surface which has a small enough area so that only a single nucleus to be grown into single crystal is formed and on which a plurality of nucleus forming surfaces each having a nucleus forming density larger than the nucleus forming density of said non-nucleus forming surface are adjacently arranged at a predetermined distance away from one another, a monocrystal is grown from the single nucleus of each of said plurality of nucleus forming surfaces which are arranged at the predetermined distance away from one another, and the grain boundary is formed at the position where said monocrystals are joined.

7. A commutator when produced directly by the method according to claim 6.

FIG. 1

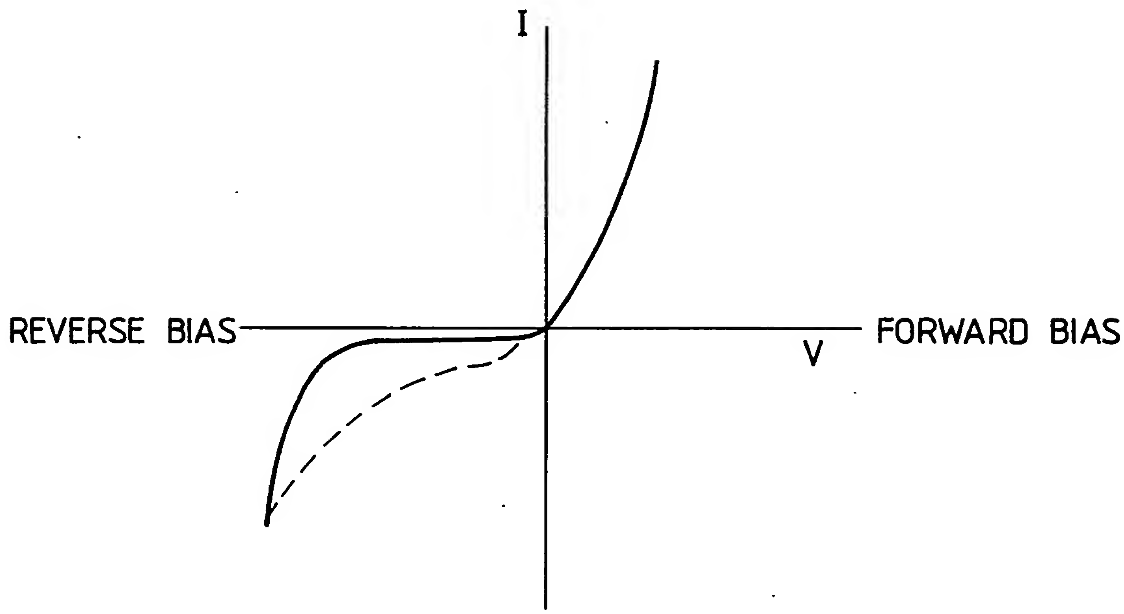



FIG. 2

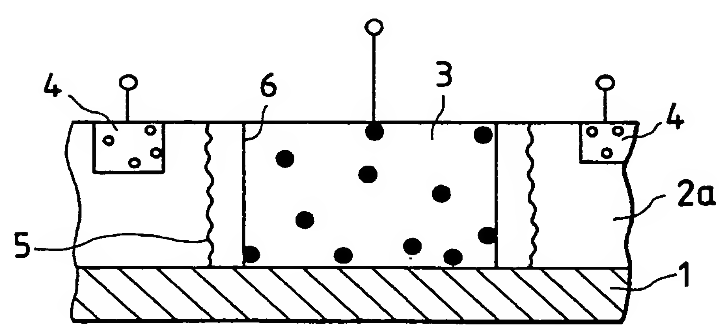


FIG. 3

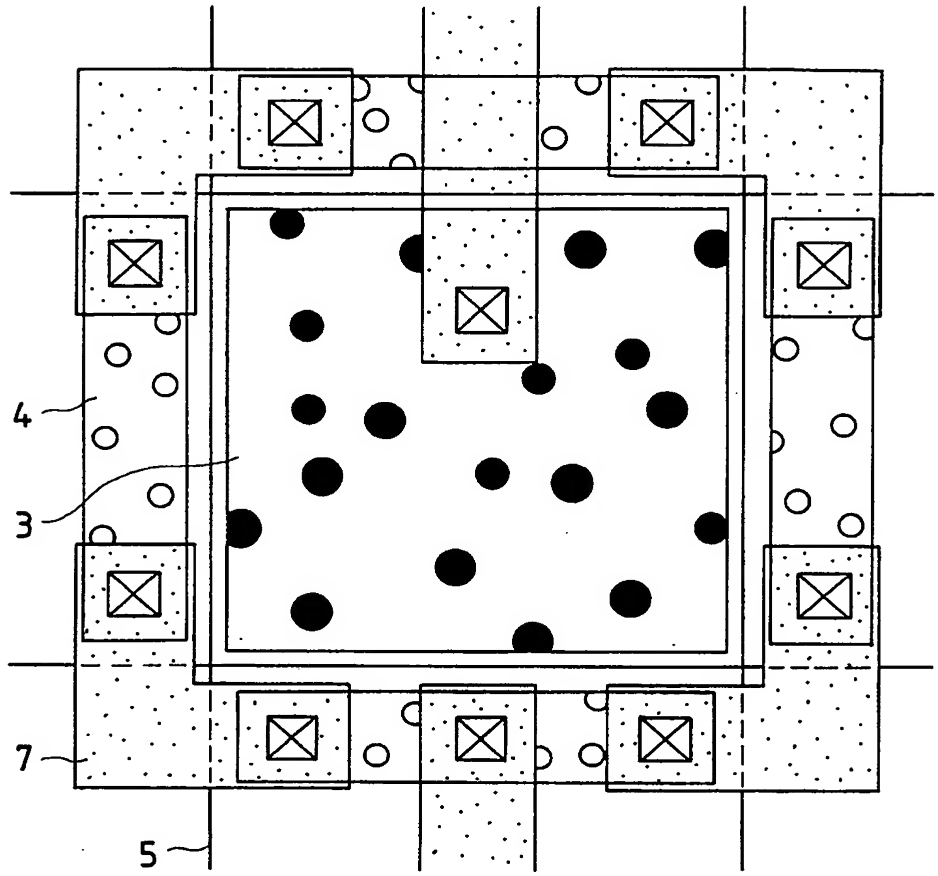



FIG. 4

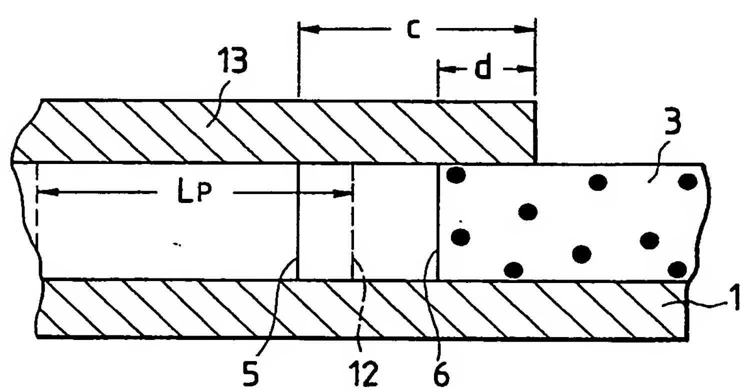


FIG. 5A

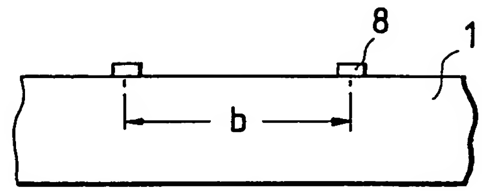



FIG. 5B

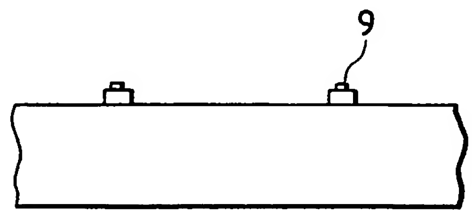



FIG. 5C

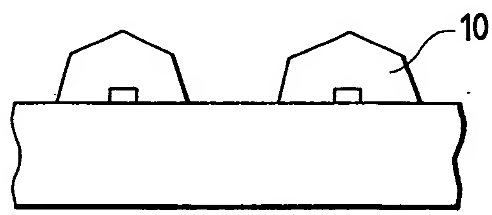



FIG. 5D

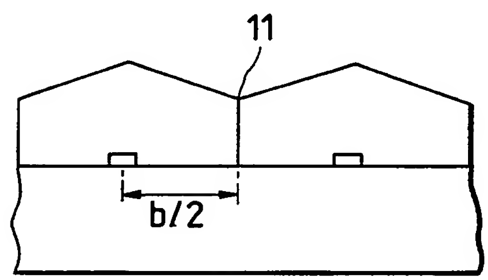



FIG. 5E

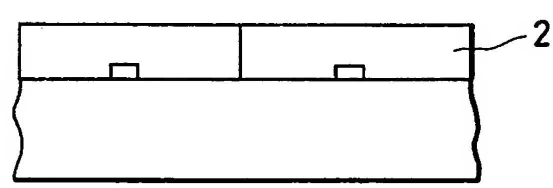


FIG. 6

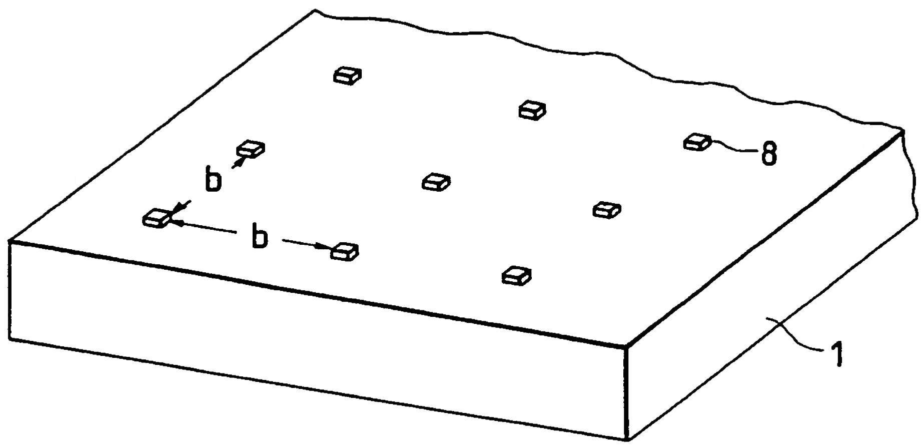



FIG. 7

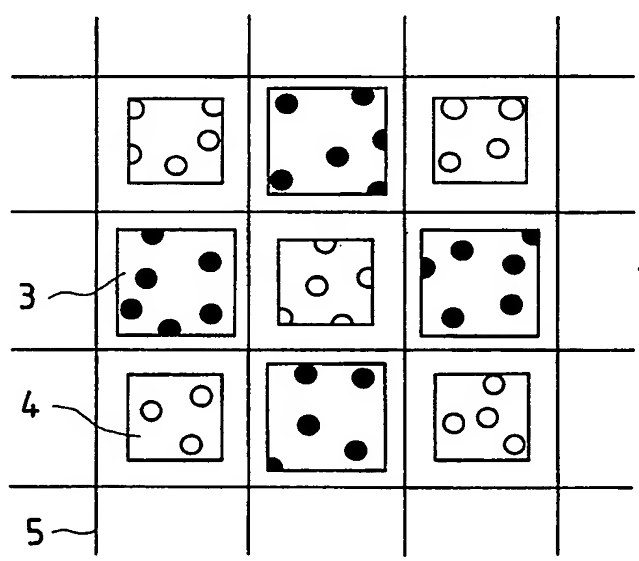


FIG. 8

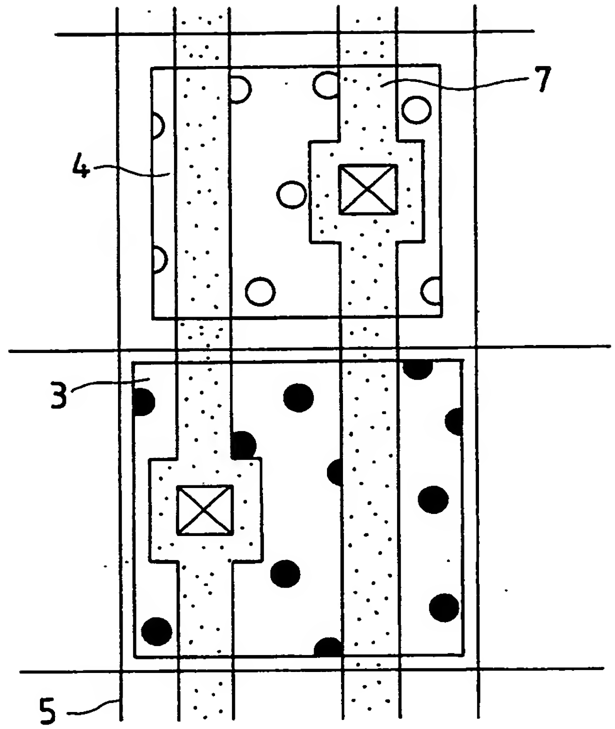
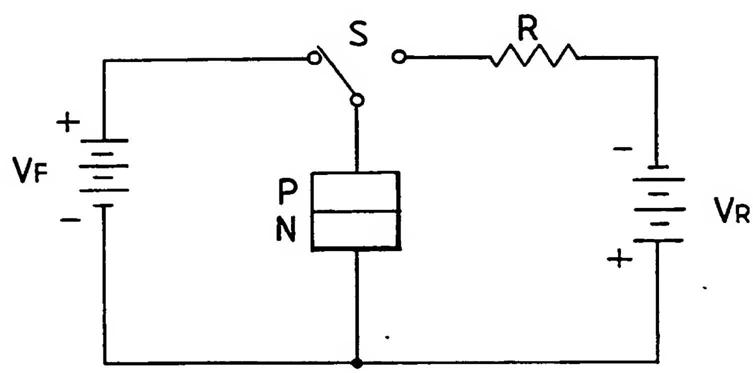



FIG. 9



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# EUROPEAN SEARCH REPORT

Application Number

EP 89 31 0727

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.5) |
|---|---|---|---|
| X | PATENT ABSTRACTS OF JAPAN, vol. 9, no. 131 (E-319)[1854], 6th June 1985; & JP-A-60 16 466 (SUWA SEIKOSHA K.K.) 28-01-1985 * Whole document * | 1,2,4,5 | H 01 L 29/91<br>H 01 L 29/30 |
| X | EP-A-0 178 447 (FUJITSU LTD) * Abstract; figure 4; page 16, line 15 - page 18, line 2 * | 1,2,4,5 | |
| A | US-A-3 900 943 (SIRTL et al.) * Abstract; figure 4; column 4, line 66 - column 5, line 16 * | 1,4,5 | |
| A | US-A-4 646 427 (OOYLE) * Abstract; figure 1; column 3, lines 1-57 * | 1,2,7 | |
| D,A | EP-A-0 244 081 (CANON K.K.) * Whole document * | 2,3,6 | |
| A | US-A-4 259 683 (ADLER et al.) * Abstract; figures 11-16; column 11, lines 5-63 * | 1,4,5 | |

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 01 L 29/90
H 01 L 29/91
H 01 L 29/04

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 12-02-1990 | MIMOUN B.J. |

CATEGORY OF CITED DOCUMENTS

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